REMARKS

Allowance of claims

Applicants note with appreciation allowance of claims 11-14, 19-38, 49-52 and 57-76 and the indication that claims 2-10, 15-18, 40-48, and 53-56 would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims.

Claim Rejections

Claim 1 has been rejected as anticipated under 35 U.S.C. 102(b) by the Koseko article entitled "Tri-state Bus Conflict Checking Method for ATPG using BDD". Claim 39, directed to a program product, has been rejected as being obvious in view of Koseko.

Applicants have carefully reviewed the Koseko paper and believe that it neither teaches nor suggests the invention of claims 1 and 39. Koseko does not even mention analyzing min-cut sets of logic which control buses in a circuit. Further, Koseko, requires the use of Binary Decision Diagrams (BDDs) which are not employed in the method of the present invention. Accordingly, Koseko cannot anticipate or render the present invention obvious.

The Invention

The present invention relates to a method for verifying proper operation of tri-state buses specified in a circuit design. The background portion of the present specification identifies a number of references, including Koseko, which attempt to achieve this objective. Each reference suffers from drawbacks which are briefly outlined. The present invention provides a method which overcomes these drawbacks in a novel and unobvious manner.

The essence of the method involves, as set forth in claim 1, "for each bus in the circuit design, performing an exhaustive analysis on a min-cut set of logic controlling the bus and designating each said bus as either conclusively conflict-free and float-free or

as inconclusive" (emphasis added). This procedure is described in detail at paragraphs 47-53 of Applicants' specification.

Test for Anticipation

The Examiner is reminded of the test for anticipation as outlined at MPEP 2131:

> "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an *ipsissimis verbis* test, i.e., identity of terminology is not required. In re Bond, 910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990). (emphasis added)

Koseko

The Koseko method involves the use of check logic and Binary Decision Diagrams (BDDs) which form no part of the claims under consideration.

The Examiner appears to rely on Figure 3 of Koseko for teachings with respect to a min-cut set of logic controlling the bus. Figure 3 was included in Koseko to show how bus outputs are connected to "check logic". There is no mention of a min-cut set of logic in the description of Figure 3 in section 3.2 of the article and no teaching that the check logic is a min-cut set of logic as claimed in the present application. Indeed, there is no reference to a min-cut set of logic anywhere in Koseko.

Koseko is addressed in paragraph 5 of Applicants' specification. As indicated therein, Koseko proposes a method which uses Binary Decision Diagrams (BDDs) to identify tri-state buses that are conflict-free and floating-free under any combination of inputs. While the method is conclusive, the method suffers from the drawback that BDDs are known to explode in size in the presence of some circuit structures such as multipliers, thus requiring excessive amounts of processing to come to a conclusion. This limitation is admitted by Koseko.

The method disclosed by Koseko appears in Section 4 entitled "Checking Procedure" (page 515) of Koseko. Step 1 involves identifying the combinational portion of the control logic of a given bus by backward tracing it from the control terminals to primary inputs and/or registers. There is no mention of identifying "a min-cut set of logic".

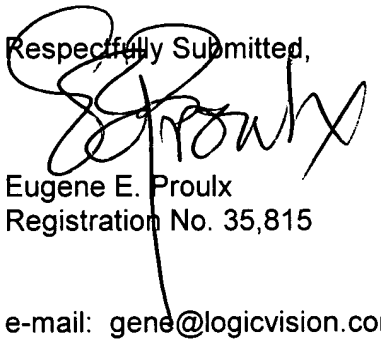
Steps 2 and 3 are steps which Applicants seek to avoid for the reasons mentioned above and in the introduction of the present specification. Step 2 calls for creating a BDD of the combinational portion of the bus control logic. Step 3 calls for creating a BDD of the check logic corresponding to the target bus. Step 4 connects the outputs of the BDD of the combinational portion of the bus control logic to the inputs of the BDD of the check logic.

Clearly, Koseko does not disclose the method claimed in claim 1 and, therefore, cannot be considered to be an anticipation of claim 1. Any suggestion that Koseko discloses the present invention can only be based on hindsight with the benefit of Applicants' specification.

Claim 39 is a program product claim which reflects the same method of claim 1 and, accordingly, distinguishes from Koseko for the same reason as claim 1.

In view of the foregoing, Koseko must be considered to fail the well established tests for anticipation and obviousness and claims 1 and 39 must be considered patentable thereover. Early favorable reconsideration and allowance of the application is respectfully requested.

Respectfully Submitted,



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